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May 11, 2004

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572 28 Davis Avenue Poughkeepsie, N.Y. 12603

Subject:

Serial No. 10/820,320 04/08/04

Yi-Hsu Wu et al.

WHOLE CHIP ESD PROTECTION

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56.

## CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on May 17, 2004.

Stephen B. Ackerman, Reg. # 37761

Signature/Date

TSMC-01-1357B

U.S. Patent 6,344,412 to Ichikawa et al., "Integrated ESD Protection Method and System," describes a method and a system for protecting integrated circuits from electrostatic discharge damage.

U.S. Patent 6,262,873 to Pequignot et al., "Method for Providing ESD Protection for an Integrated Circuit," discloses a method for providing electrostatic protection for integrated circuits.

U.S. Patent 6,218,704 to Brown et al., "ESD Protection Structure and Method," discloses an integrated circuit structure and method for electrostatic discharge protection for chips.

Sincerely,

Stephen B. Ackerman,

Reg. No. 37761

citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.